**Module 3: The Arm Cortex-M0 Processor Architecture: Part 2**

1. Which of the following instructions will cause the processor to go into sleep mode?

1. DMB
2. WFE
3. NOP
4. SVM

2. When you execute the following instruction:

STR R1, [R2]

this may cause:

1. the contents of R1 to be modified
2. the contents of R2 be modified
3. the contents of both R1 and R2 to be modified
4. None of the above.

3. Which of the following instructions are 32-bit Thumb-2 instructions?

1. BL
2. WFI
3. TST
4. SVC

4. Which of the following branch instructions is conditional? (There may be more than one correct answer.)

1. BEQ R2
2. BX R1
3. BLE R1
4. BLX R0

5. Which of the following instructions is only used in multiprocessor systems?

1. SEV
2. SVC
3. DMB
4. ISB

6. Which of the following registers do you need to modify to enable/disable sleep features?

1. Interrupt mask special register
2. Program status register
3. Link register
4. System control register

7. Which of the following branch instructions will change the value of the link register?

1. BEQ R2
2. BLX R1
3. BLE R1
4. None of the above.

8. Endian refers to the order of bytes stored in memory. Cortex-M0 supports two styles of endian: big and small. Which of the following instructions can be used for conversion of data items from a big endian to a small endian format?

1. REV
2. ROROS
3. BTS
4. ROS